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Substitute for form 1449A/B/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>				Complete if Known	
				Application Number	10/801,308-Conf. #2000
				Filing Date	March 16, 2004
				First Named Inventor	Koji Hirairi
				Art Unit	2127
				Examiner Name	Not Yet Assigned
				Attorney Docket Number	SCEI 3.0-178
Sheet	1	of	1		

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
	AA*	US-2002/0053684-A1	05/2002	Chauvel et al.	
	AB*	US-2002/0065049-A1	05/2002	Chauvel et al.	
	AC*	US-2003/0125900-A1	07/2003	Orenstien et al.	
	AD*	US-5,274,797	12/1993	Barlow et al.	
	AE*	US-5,715,184	02/1998	Tyler et al.	
	AF*	US-5,761,516	06/1998	Rostoker et al.	

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
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NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	CA	Skadron et al., "Temperature-Aware Microarchitecture: Modeling arid Implementation," ACM trans-on architecture and Code optimization, pp. 94-125, March 2004.	
	CB	Azevedo et al., "Architectural and Compiler Strategies for Dynamic Power Management in the COPPER Project," 2001 International Workshop on Innovative Architecture, January, 2001. -	
	CC	Heo et al., "Reducing Power Density through Activity Migration," Proceedings of the 2003 International Symposium on Low Power Electronics and Design (ACM Press, ©2003), pp. 217-222.	
	CD	Tiwari et al. "Instruction Level Power Analysis and Optimization of Software," Journal of VLSI Signal Processing, Vol. 13, No.2 (August 1996), pp. 1-18.	
	CE	Abhishek Mehta, 'Techniques for Low Power Processing - A Survey' CSE 822, Spring 2001, A29838087, Retrieved from the Internet on March 29, 2004, cURL: w~w.cs.vcr.edu/~chzhanp/paners_read/lowpower_survey.pdf ; 10 pages.	-
	CF	Lee et al., "Power Analysis and Minimization Techniques for Embedded DSP Software," IEEE Transactions on VLSI Systems, Vol. 5, No. 1, March 1997, pp. 123-135 (manuscript copy submitted).	
	CG	Gerosa et al., "A 250-MHz 5-W PowerPC Microprocessor with On-Chip 1.2 Cache Controller," IEEE Journal of Solid-State Circuits, Vol. 32, No. 11, November 1997, pp. 1635-1649.	-

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